AD8348 Evaluation Board

EVAL-AD8348EB

BOARD DESCRIPTION

Figure 1 shows the schematic for the EVAL-AD8348EB. Note that uninstalled components are indicated with the OPEN designation. The board is powered by a single supply in the range of 2.7 V to 5.5 V. Table 1 details the various configuration options of the evaluation board. Table 2 shows the various jumper configurations for operating the evaluation board with different signal paths.

Power to operate the board can be fed to a single $+V_S$ test point located near the LO input port at the top of the evaluation board. A GND test point is conveniently provided next to the $+V_S$ test point for the return path.

The device is enabled by moving Switch SW11 (at the bottom left of the evaluation board) to the ENBL position. The device is disabled by moving SW11 to the DENBL position. If desired, the device can be enabled and disabled from an external source that can be fed into the ENBL SMA connector or the VENB test point, in which case SW11 should be placed in the DENBL position.

The IF and MX inputs are selected via SW12. The switch should be moved in the direction of the desired input.

For convenience, a potentiometer, R15, is provided to allow for changes in gain without the need for an additional dc voltage source. To use the potentiometer, the SW13 switch must be set to the POT position. Alternatively, an external voltage applied to either the test point or SMA connector labeled VGIN can set the gain. SW13 must be set to the EXT position when an external gain control voltage is used.

The local oscillator signal should be fed to the SMA connector J21. This port is terminated in 50 Ω. The LO power input range is from –12 dBm to 0 dBm and at a frequency equal to double that of the IF/MX frequency.

The IF input should be fed into the SMA connector IFIP. The VGA must be enabled when this port is used (SW12 in the IF position).

The EVAL-AD8348EB is by default set for differential MX drive through a balun (T41) from a single-ended source fed into the MXIP SMA connector. To change to a differential driving source, T41 should be removed along with Resistor R42. The 0 Ω Resistors R43 and R44 should be installed in place of T41 to bridge the gap in the input traces. This will present a nominal differential impedance of 200 Ω (100 Ω each side). The differential inputs should then be fed into SMA connectors MXIP and MXIN.

The baseband outputs are made available at the IOPP, IOPN, QOPP, and QOPN test points and SMA connectors. These outputs are not designed to be connected directly to 50 Ω loads and should be presented with loads of approximately 2 kΩ or more.

The dc bias level of the baseband amplifier outputs are by default tied to VREF through LK11. If desired, the dc bias level can be changed by removing LK11 and driving a dc voltage onto the VCMO test point.

ORDERING GUIDE

AD8348 Products	Package Description
AD8348-EVAL	Evaluation Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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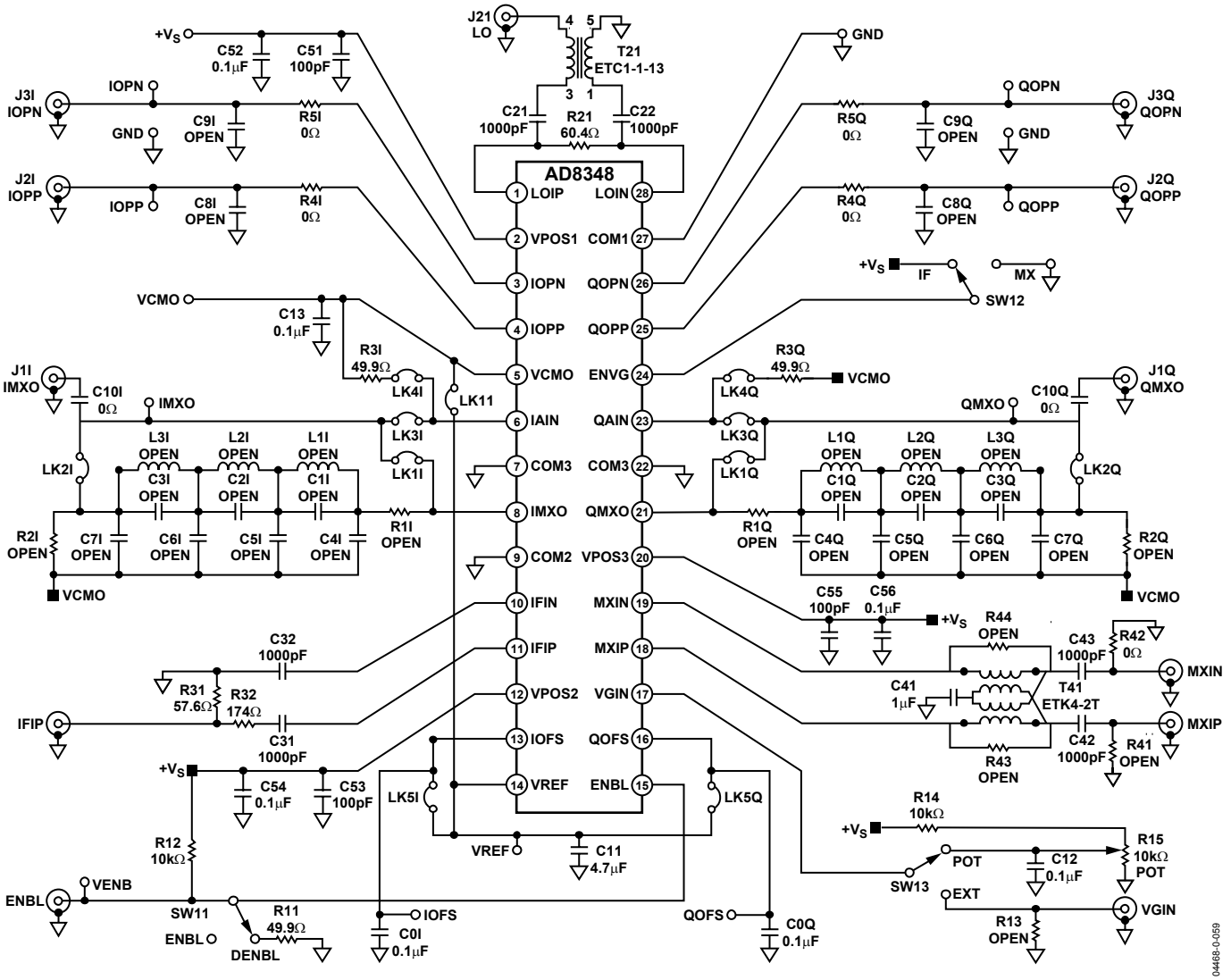

Figure 1. Evaluation Board Schematic

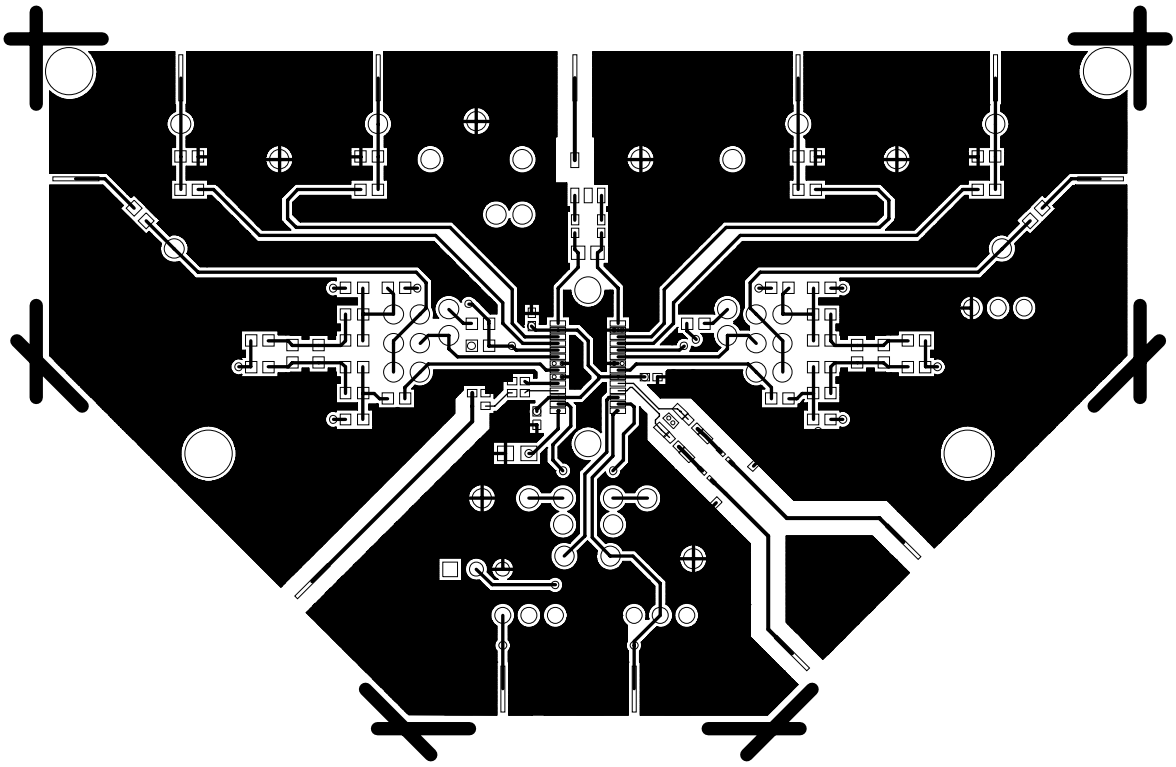

Figure 2. Evaluation Board Top Layer

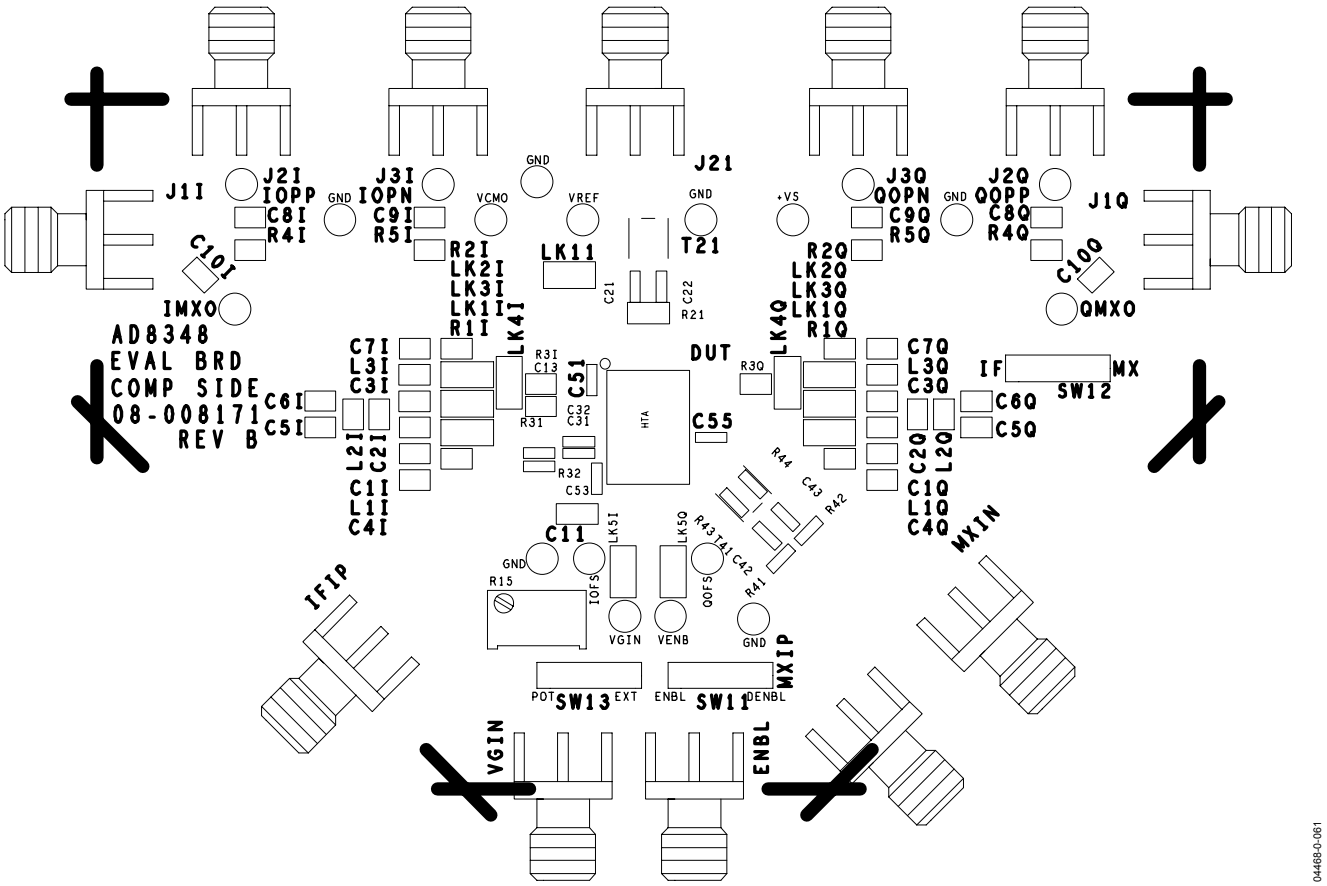

Figure 3. Evaluation Board Top Silkscreen

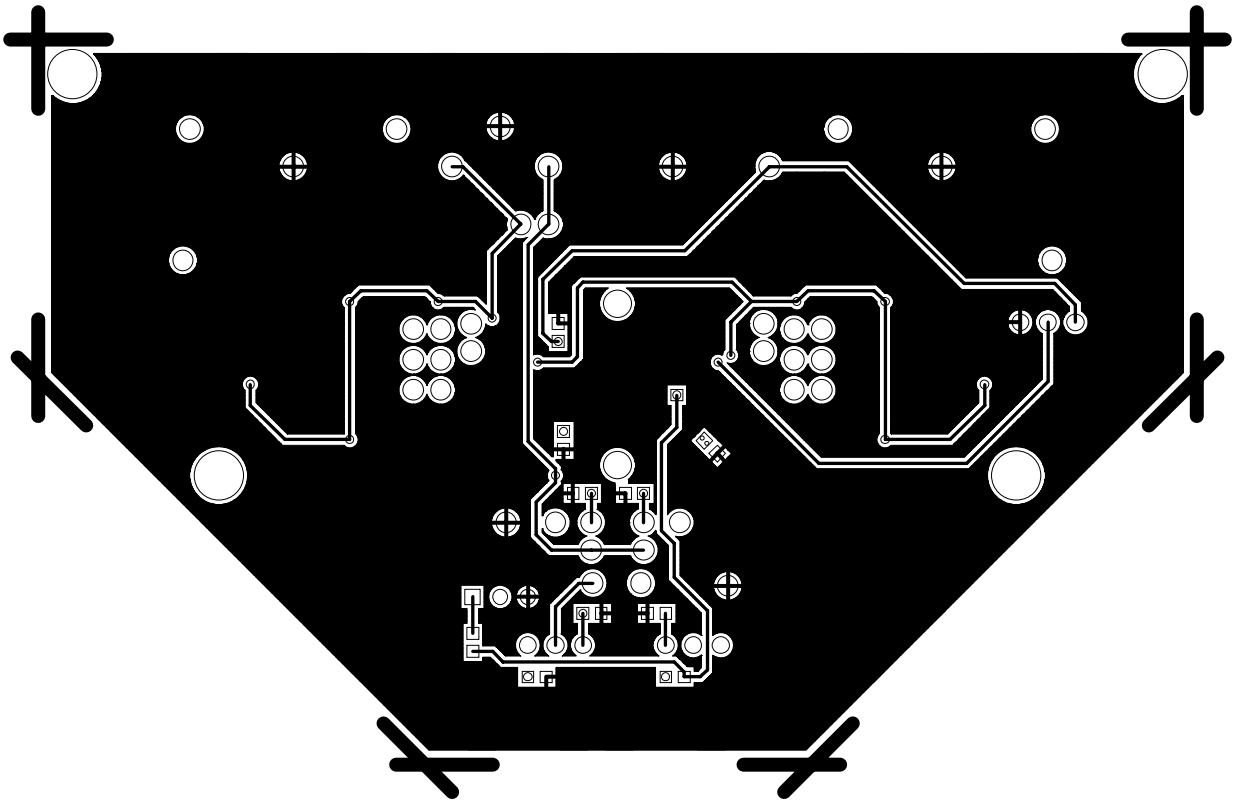

Figure 4. Evaluation Board Bottom Layer

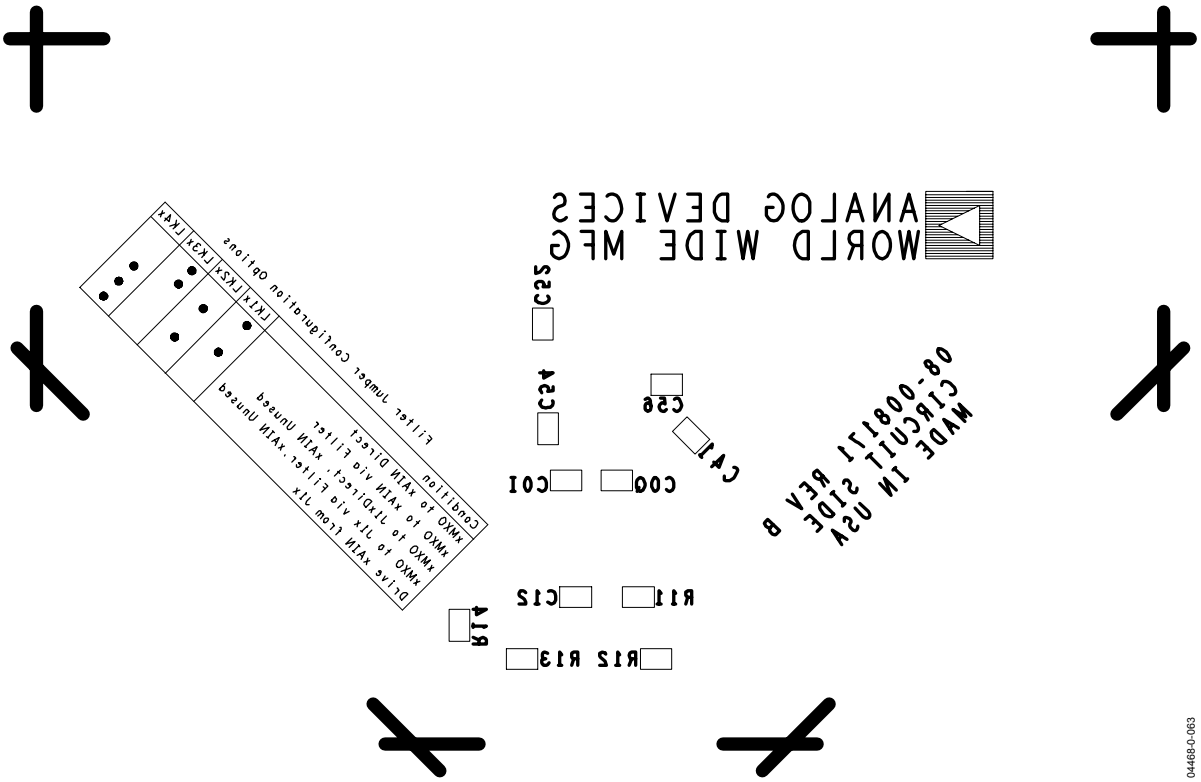

Figure 5. Evaluation Board Bottom Silkscreen

Table 1. Evaluation Board Configuration Options

Component	Function	Default Condition
$+V_S$, GND	Power Supply and Ground Vector Pins.	Not Applicable
SW11, ENBL	Device Enable. Place SW11 in the ENBL position to connect the ENBL pin to $+V_S$. Place SW11 in the DENBL position to disable the device by grounding the ENBL pin through a 50 Ω pull-down resistor. The device may also be enabled via an external voltage applied to ENBL or VENB.	SW11 = ENBL
SW13, R15, VGIN	Gain Control Selection. With SW13 in the POT position, the gain of the VGA can be set using the R15 potentiometer. With SW13 in the EXT position, the VGA gain can be set by an external voltage to the SMA connector VGIN. For VGA operation, the VGA must first be enabled by setting SW12 to the IF position.	SW2 = POT
SW12	VGA Enable Selection. With SW12 in the IF position, the ENVG pin is connected to $+V_S$ and the VGA is enabled. The IF input should be used when SW12 is in the IF position. With SW12 in the MX position, the ENVG pin is grounded and the VGA is disabled. The MX inputs should be used when SW12 is in the MX position.	SW12 = IF
IFIP, R31, R32	IF Input: The single-ended IF signal should be connected to this SMA connector. R31 and R32 form an L Pad that presents a 50 Ω termination to the input.	R31 = 57.6 Ω R32 = 174 Ω
MXIP, MXIN T41, R41, R42, C42, C43	Mixer Inputs. These inputs can be configured for either differential or single-ended operation. The evaluation board is by default set for differential MX drive through a balun (T41) from a single-ended source fed into the MXIP SMA connector. To change to a differential driving source, T41 should be removed along with Resistor R42. The 0 Ω Resistors R43 and R44 should be installed in place of T41 to bridge the gap in the input traces. This will present a nominal differential impedance of 200 Ω (100 Ω each side). The differential inputs should then be fed into SMA connectors MXIP and MXIN.	T41 = M/A-COM ETK4-2T R41, C42, C43 = OPEN R42 = 0 Ω
LK11, VCMO	Baseband Amplifier Output Bias. Installing LK11 connects VREF to VCMO. This sets the bias level on the baseband amplifiers to VREF, which is equal to approximately 1 V. Alternatively, with LK11 removed, the bias level of the baseband amplifiers can be set by applying an external voltage to the VCMO test point.	LK11 Installed
C8, C9, R4, R5 (I and Q)	Baseband Amplifier Outputs and Output Filter. Additional low-pass filtering can be provided at the baseband output with these filters.	R4, R5 = 0 Ω
C10 (I and Q)	Mixer Output DC Blocking Capacitors. The mixer outputs are biased to VCMO. To prevent damage to test equipment that cannot tolerate dc biases, C10 is provided to block the dc component, thus protecting the test equipment.	C10 = 0 Ω
C1–C7 R1, R2 L1–L3 (I and Q)	Baseband Filter. These components are provided for baseband filtering between the mixer outputs and the baseband amplifier inputs. The baseband amplifier input impedance is high and the filter termination impedance is set by R2. See Table 2 for the jumper settings.	All = OPEN
LK5 (I and Q)	Offset Compensation Loop Disable. Installing these jumpers will disable the offset compensation loop for the corresponding channel.	LK5x = OPEN

Table 2. Filter Jumper Configuration Options

Condition	LK1x	LK2x	LK3x	LK4x
xMXO to xAIN Direct	•		•	
xMXO to xAIN via Filter		•	•	
xMXO to J1x Direct, xAIN Unused	•			•
xMXO to J1x via Filter, xAIN Unused		•		•
Drive xAIN from J1x				•

NOTES

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